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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,024	10/24/2003	Karsten Wieczorek	2000.108600	1749

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,024	WIECZOREK ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/9/04;7/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Aronowitz et al. (U.S. Patent No. 6,033,998).

4. As to claim 1, Aronowitz discloses a method of forming an insulating layer, the method comprising: forming a dielectric layer (206) (column 5, lines 58-59) with an initial thickness on an oxidizable substrate (200) (column 5, lines 44-47); introducing nitrogen into said dielectric layer (206) (column 6, lines 3-5); and locally increasing said initial thickness of said dielectric layer (206) according to a local nitrogen concentration (column 6, lines 61-67; column 7, lines 1-6).

5. As to claim 2, Aronowitz discloses that said initial thickness is locally increased by oxidizing said substrate (column 5, lines 58-59).

6. As to claim 3, Aronowitz discloses that said dielectric oxide layer (206) comprises silicon dioxide (column 5, lines 58-59) and the initial thickness is in the range of approximately 0.5-5 nm (column 5, lines 61-63).

7. As to claim 4, Aronowitz discloses determining a ratio of said initial thickness and a maximum local increase to control a specific characteristic of said insulating layer (column 7, lines 1-13).

8. As to claim 5, Aronowitz discloses that said ratio is determined as a target value in advance (column 7, lines 10-13).

9. As to claim 6, Aronowitz discloses that said ratio is achieved by controlling at least one of said initial thickness (column 5, lines 61-63), a process parameter while locally increasing said initial thickness (column 6, lines 61-67; column 7, lines 1-6), and a process parameter while introducing said nitrogen (column 6, lines 55-60).

10. As to claim 7, Aronowitz discloses that said dielectric layer is formed by at least one of thermal growth, rapid thermal oxidation, chemical vapor deposition, atomic layer deposition and chemical reaction (column 5, lines 58-61).

11. As to claim 8, Aronowitz discloses patterning said insulating layer as a plurality of gate insulation layers (206a/206b) (column 5, lines 64-65) for PMOS transistors (column 1, lines 33-34, lines 63-67; column 2, lines 1-10) at different locations on said substrate.

12. As to claim 9, Aronowitz discloses that said nitrogen is introduced into said insulating layer by exposing said substrate to a nitrous plasma (column 6, lines 6-28).

13. As to claim 10, Aronowitz discloses a method, comprising: forming a silicon dioxide layer (206) as a base layer for a gate dielectric with an initial thickness on a first

area (206a) and a second area (206b) of a silicon containing semiconductor layer provided on a substrate (column 5, lines 58-65); introducing nitrogen into said silicon dioxide layer (column 6, lines 3-5); and increasing said initial thickness in said first and second areas on the basis of a nitrogen concentration contained therein and a desired characteristic of said gate dielectric (column 6, lines 61-67; column 7, lines 1-6).

14. As to claim 11, Aronowitz discloses that increasing said initial thickness includes oxidizing said substrate (column 5, lines 58-59).

15. As to claim 12, Aronowitz discloses that oxidizing said substrate is performed after introducing nitrogen into said silicon dioxide layer (column 6, lines 61-67; column 7, lines 1-6).

16. As to claim 14, Aronowitz discloses determining a ratio of said initial thickness and a maximum thickness increase in one of said first (206a) and second areas (206b) to control a specific characteristic of said gate dielectric (column 7, lines 10-13; Table I, column 7, lines 35-49).

17. As to claim 15, Aronowitz discloses that said ratio is determined as a target value in advance (column 7, lines 10-13; Table I, column 7, lines 35-49).

18. As to claim 16, Aronowitz discloses that said ratio is achieved by controlling at least one of said initial thickness (column 5, lines 61-63), a process parameter while locally increasing said initial thickness (column 6, lines 61-67; column 7, lines 1-6), and a process parameter while introducing said nitrogen (column 6, lines 55-60; Table I, column 7, lines 35-49).

19. As to claim 17, Aronowitz discloses said silicon dioxide layer is formed by at least one of thermal growth, rapid thermal oxidation, chemical vapor deposition, atomic layer deposition and chemical reaction (column 5, lines 58-61).

20. As to claim 18, Aronowitz discloses patterning said gate dielectric layer as a plurality of gate insulation layers (206a/206b) (column 5, lines 64-65) for PMOS transistors (column 1, lines 33-34, lines 63-67; column 2, lines 1-10) at different locations on said substrate.

21. As to claim 19, Aronowitz discloses that nitrogen is introduced into the base layer by exposing said substrate to a nitrous plasma (column 6, lines 6-28).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz.

24. As to claim 13, Aronowitz does not expressly disclose that wherein oxidizing said substrate is performed at least partially simultaneously with introducing nitrogen into said silicon dioxide layer. Aronowitz discloses two discrete process steps for introducing nitrogen into silicon dioxide layer (206) (column 6, lines 3-6) and oxidizing the substrate (column 6, lines 61-62). However, Aronowitz teaches limiting the number of high temperature treatment steps involved in processing (column 2, lines 23-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of oxidizing said substrate at least partially simultaneously with introducing nitrogen into said silicon dioxide layer. One who is skilled in art would be motivated to limit the overall thermal budget in processing the device and to reduce the number of process steps.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hu et al. (U.S. Patent Appl. Pub. No. 2003/0080389) discloses exposing an oxide layer to nitrogen, followed by a second oxidation step. Ma et al. (U.S. Patent No. 6,207,586) discloses forming an oxide/nitride stacked layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
June 2, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER